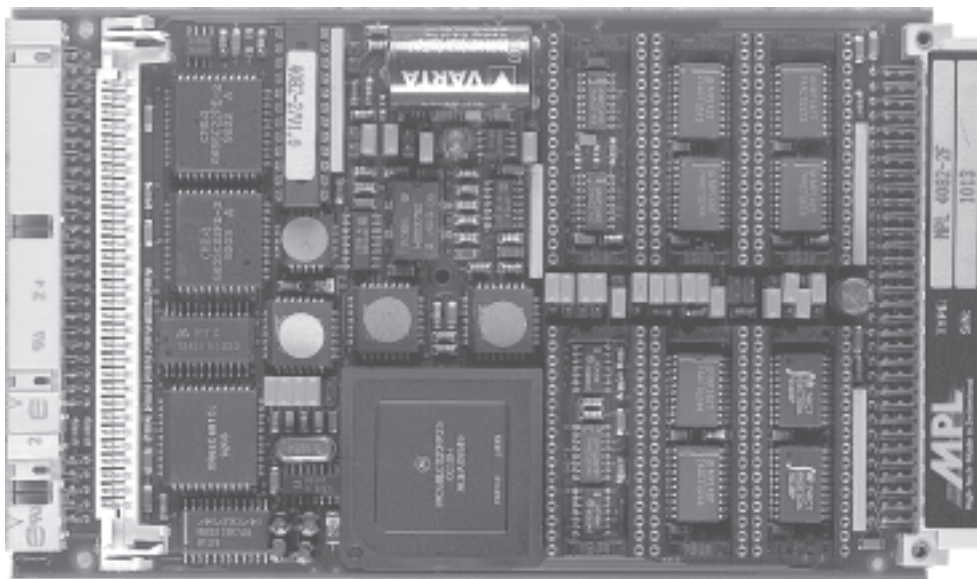


HIGH FUNCTIONALITY CMOS 68EC020 SINGLE BOARD COMPUTER

The MPL 4082 is the industry's most integrated, all CMOS 68EC020 32-bit single board computer, and has an impressive list of features: six 32-pin sockets organized in two banks for SRAM and EPROM allow up to 3 Mbytes of internal memory, on-board battery for buffering of SRAM and RTC, serial and parallel I/O's, Real Time Clock with calendar, Watchdog, Power fail detection and serial EEPROM. With an optional floating-point coprocessor 68882, computing and calculation power can be upgraded by factors. The MPL 4082 can be further customized with the use of a miniature 30-pin connector for additional mounting of SIMM Modules (small PCBs). The board also supports a full 16-bit G-64/G-96 bus interface for I/O extension and up to 12 Mbytes of external memory. The fully CMOS architecture and its single-supply design draws a mere 300mA on 5V only and makes the MPL 4082 ideal for a wide range of control, data acquisition, and portable microcomputer applications.

TECHNICAL FEATURES

- Powerful 32-bit 68EC020
- 16 MHz clock (25 MHz optional)
- 68882 Floating-Point Coprocessor (optional)
- Two memory banks allow up to 3 Mbytes of internal memory
- Up to 2 Mbytes of battery buffered SRAM
- Up to 2 Mbytes of EPROM
- JEDEC pin out for 256 kbit to 4 Mbit EPROM/SRAM devices
- 1024 bit serial EEPROM included
- Two programmable RS-232 serial ports
- 40 TTL I/O lines
- Five 16-bit timers
- Real-time clock with calendar
- Powerfail detection
- Comfortable watchdog
- Level 7 interrupt sources are detectable
- Full G-64/G-96 bus interface
- External memory expandable up to 12 Mbytes (VMA)
- Supports sync. and async. I/O transfers (VPA)
- Active bus-DTACK locks next bus access
- Bus arbitration capability
- On-board MLX SIMM local extension bus
- All CMOS design
- Very low power consumption: 300mA typ. at 5V only
- Compact single height Eurocard design (100 x 160 mm)
- 6-level multilayer design
- Comprehensive software support
- Available in extended temperature range



References :

- MPL 4082-2 68EC020 single board computer, 16 MHz
- MPL 4082-2F 68EC020 single board computer, 25 MHz
- MPL 4082-2X 68EC020 single board computer, 16 MHz, -25 to +85°

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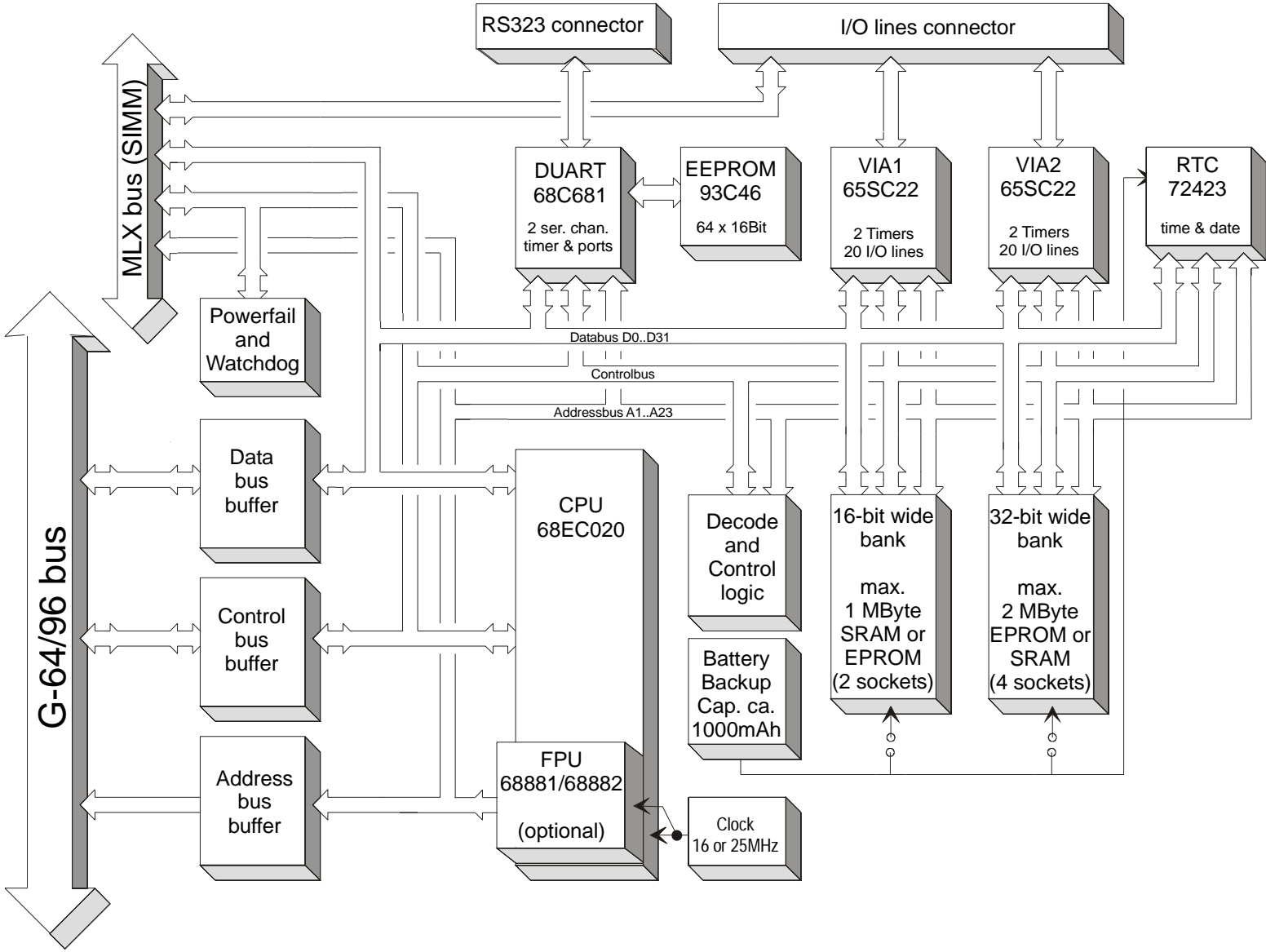


Fig. 1.1 MPL 4082 block diagram

1. GENERAL INFORMATION

1.1 DESCRIPTION

The MPL 4082 is a high density single board computer, built in all CMOS low power technology around a 32-Bit 68EC020 running at 16 MHz (25 MHz available optionally). The 68EC020 is Motorola's economical successor of the earlier introduced 68020. The only differences between these family members are the reduced addressing range (down to 24-bit) and some omitted control signals. The 68EC020 core is compatible to the 68020 core and therefore the 68EC020 offers the same features and performance as known from the 68020: Eighteen addressing modes, optimized instruction set, on-chip instruction cache, dynamic bus sizing and a coprocessor interface. The performance level of the 68EC020 guarantees excellent processing power and satisfies the requirements of very sophisticated applications based on high-level languages.

The floating-point coprocessor 68882 instruction set is a natural extension to the 68EC020. The 68882 can be equipped optionally by use of a small and compact piggy back and increases calculating power of the MPL 4082 by factors. The 68882 runs on the same clock as the 68EC020.

The MPL 4082 is loaded with features that makes it one of the most flexible and most versatile single board computers in the market. The board contains six JEDEC sockets that can be equipped with up to 3 Mbytes of SRAM and EPROM. The on-board memory is split into two banks where the first bank is 16-bit wide with a memory space of 1 Mbyte and the second bank is 32-bit wide with 2 Mbyte memory space. The MPL 4082 supports two memory maps. One with EPROM mounted on the 16-bit bank and SRAM on the 32-bit bank and a second map vice versa. This feature allows to select a memory configuration matching the requirements of your application program, with optimized access speed and memory distribution. The whole SRAM can be battery backed up using an on-board lithium battery. A 1024 bit serial access EEPROM allows the permanent storage of useful operating parameters. In addition, the MPL 4082 is equipped with two RS-232 serial ports, 40 TTL I/O lines, five 16 Bit timers, a Real Time Clock with calendar, and a Power-fail detection and Watchdog circuit. The Watchdog can be enabled by software which allows applications with long lasting start-up procedures. All internal 8-bit peripherals are assumed to be 16-bit wide and are connected to the odd byte. This makes the MPL 4082 very similar to the MPL-4080, an earlier 68HC000 CPU-board from MPL AG, and makes the porting of software from one board to the other a simple operation.

For additional memory and I/O, the board can be extended by 12 megabytes through its G-64/96 bus interface. A special bus circuit monitors the bus DTACK and delays the start of bus accesses as long as the bus DTACK stays active. The G-64/96 bus is a favorite 16/32-bit bus architecture among OEMs of embedded computer systems. A really exciting feature of the MPL 4082 is its use of a 30 pin. SIMM (Single Inline Multipurpose Module) microedge connector to accept small PCBs mounted at a 30 degree angle for the purpose of installing

additional I/O to the board. All relevant signals to operate 8-bit peripherals are available on that connector. MPL AG is offering a range of SIMM add-on modules. Available today (Feb 1993) is a module containing a 12-bit A/D and D/A converter, three serial modules and a CAN (Controller Area Network) module covering different customer needs.

Software development on the MPL 4082 is simplified by the availability of the OS-9 real-time, multitasking operating system. MPL AG also supplies software allowing cross development using an IBM PC for OS-9 (PC-Bridge) or for stand alone applications (CrossCode C). The MPL 4082 fills an important need for high performance, ruggedized extended temperature, low power microcomputer systems for application in transit systems, portable instruments and testers, and remote data acquisition systems.

1.2 TECHNICAL CHARACTERISTICS

Processor:	68EC020
Processor clock:	16 MHz clock (25 MHz optional)
Coprocessor:	68882 (optional)
Memory:	
JEDEC sockets:	6 x 32-pin
Max. Memory:	3 Mbyte
Equipped memory:	Up to 2 Mbyte SRAM Up to 2 Mbyte EPROM 1024 Bit serial EEPROM
Serial ports:	
Nb of ports:	Two RS-232C (68C681)
Baud rate:	50 - 38400, software programmable
TTL I/O:	40 digital I/O lines with TTL-Level (two 65SC22)
Clock/timers:	
Timers:	Five 16-bit timers
Clock/Calendar:	RTC72423, battery buffered
Bus interface:	
Interface type:	Full G-64/96
Ext. Mem. Addressing:	12 Mbytes (VMA)
Memory transfers:	Asynchronous
I/O Addressing:	1 kword (VPA)
I/O transfers:	Sync./Async.
Enable clock:	CPU clock / 16
Bus arbitration:	Supported
G-96-Interrupts:	3 auto-vectored 2 vectored

Local Expansion: Bus Name: Connector type: Bus Type:	(MLX) Mpl Local eXpansion 30-pin SIMM 8-bit synchronous
Board Dimensions:	Single Eurocard (100 x 160mm)
Technology:	100% CMOS Surface Mounted Devices
Power requirements: Power range:	+ 5V only / 300mA with RAM/EPROM (16MHz) 4.80V - 5.25V
Temperature range: MPL-4080-X version: Relative humidity:	0° to +70°C (+32° to +158°F) -25° to +85°C (-13° to +185°F) 20-90% non condensing

Table 1.2: Technical characteristics

1.3 POWER CONSUMPTION

The fully CMOS-design of the MPL 4082 results in a low power consumption. The power values as documented in table 1.3, have been determined under the following conditions: Supply of 5.0 volts, four 1 Mbit CMOS SRAMs (32-bit wide), two 1 Mbit CMOS EPROMs (16-bit wide), serial communication on one channel, cache enabled and the MPL 4082 is *not* mounted on a bus backplane.

The typical values for the idle/processing state at different frequencies and temperatures are shown in table 1.3.

Temp.	16 MHz		25 MHz	
	CPU 100% idle	CPU 100% prc.	CPU 100% idle	CPU 100% prc.
-25°	255mA	315mA	290mA	385mA
+25°	240mA	300mA	275mA	370mA
+85°	225mA	285mA	260mA	355mA

Table 1.3 Power consumption

2. PREPARATION FOR USE, INTERCONNECTION

2.1 PARTS LOCATION

The diagram of Fig. 2.1 shows the position of all components, jumpers and connectors on the MPL 4082.

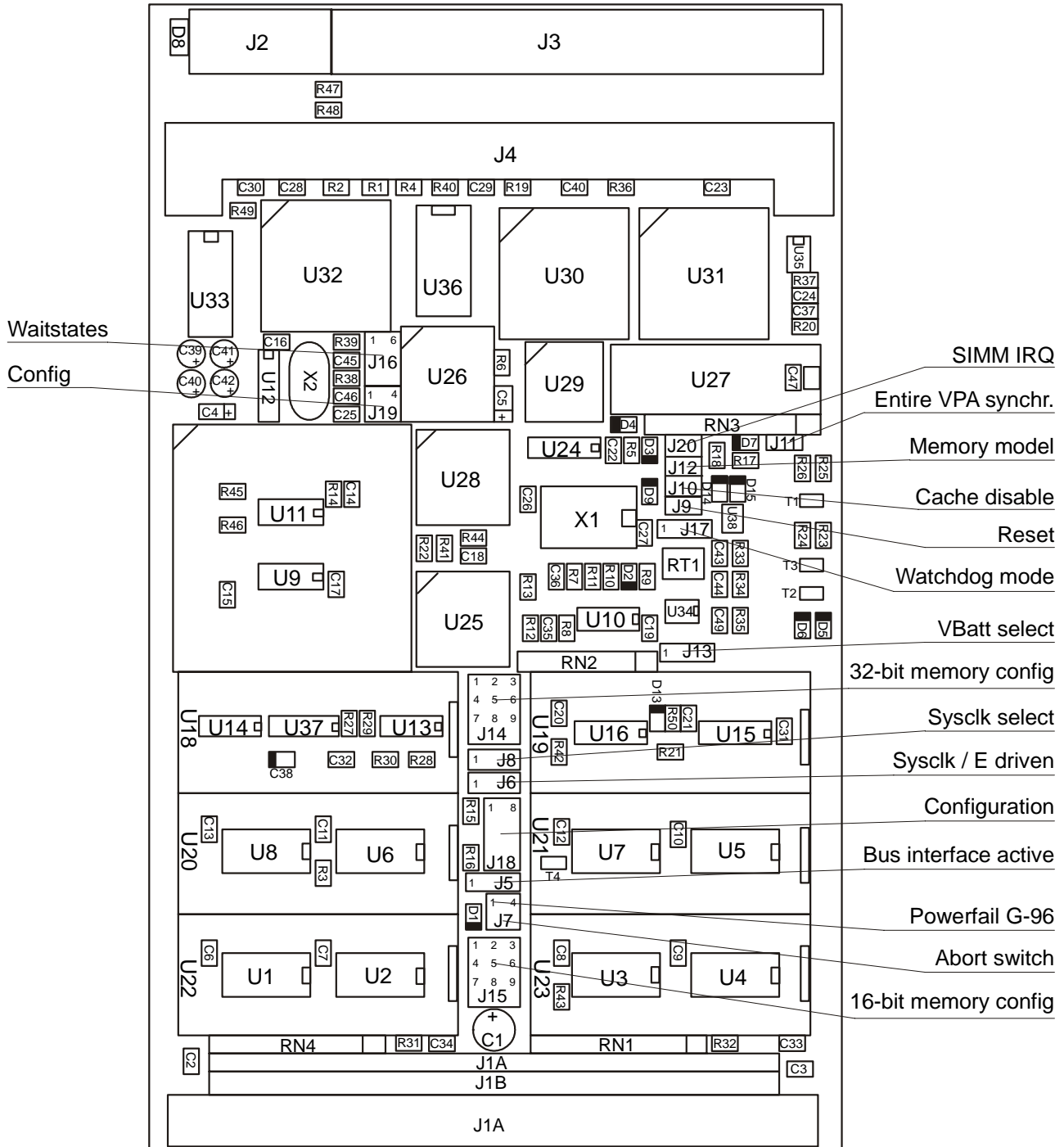


Fig. 2.1 MPL 4082 parts location

2.1.1 JUMPER AND CONNECTOR OVERVIEW

Name	Function
J1	G-96 connector
J2	Dual RS-232 10pol connector
J3	I/O lines 50pol connector
J4	SIMM microedge 30pol connector
J5	G-96 address bus drivers control
J6	Enable and SYCLK control
J7	Abort/PWF-G-96 jumper
J8	SYCLK frequency selection
J9	Reset
J10	Cache enable/disable
J11	Sync. or async.VPA-range selection
J12	Memory map selection
J13	Battery source selection
J14	Type and size of memory on 32-bit bank
J15	Type and size of memory on 16-bit bank
J16	Memory wait states
J17	Soft/hardware clear of the watchdog
J18	4-bit configuration
J19	2-bit configuration
J20	SIMM Module interrupt

Table 2.1 Jumper and connector assignment

2.2 ALL ABOUT MEMORY AND BANKS

All information necessary for correct installation and jumpering of the on-board memory can be found in this paragraph.

2.2.1 JUMPER ORIENTATION

A special feature of the MPL 4082 helps to check misplaced jumpers: All jumpers have to be parallel to the G-96 connector (this does not exclude additional mis-jumpering).

2.2.2 MEMORY BANKS

The internal memory of the MPL 4082 is organized in two banks. The first bank is 16-bit wide, connected to CPU data lines D16 to D31, consists of two 32 pin sockets and offers a memory space of 1 Mbyte. The second bank is 32-bit wide, connected to CPU data lines D0 to D31, consists of four 32 pin sockets and offers a memory space of 2 Mbytes. All these parameters cannot be changed since they are fixed in hardware.

See figure 2.2 for physical bank location and byte association within the banks.

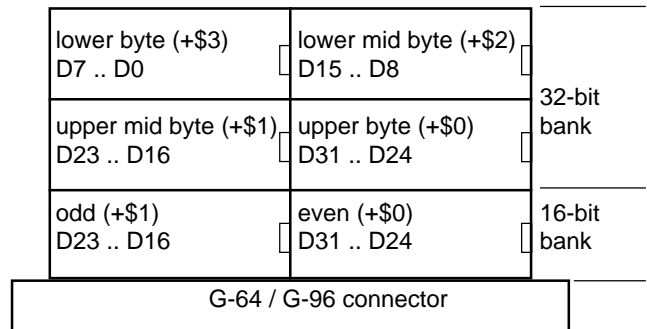


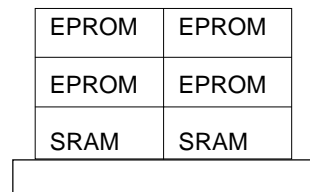
Figure 2.2 Bank location and byte association

2.2.3 MEMORY MAP SELECTION (J12)

Each bank can be equipped with SRAM or EPROM, but if SRAM is equipped on the 16-bit bank, then EPROM has to be equipped on the 32-bit bank and vice versa. This results in two memory configurations (maps). Switching between the two maps is done by jumper J12. Both maps have in common that EPROM always starts at address \$000000. The two memory maps are explained in table 2.3.

— J12 = 'out' —

Type	Space	Range	Bank
SRAM	1 Mbyte	200000 2FFFFFF	16-bit bank
EPROM	2 Mbyte	000000 1FFFFFF	32-bit bank



— J12 = 'in' —

Type	Space	Range	Bank
SRAM	2 Mbyte	100000 2FFFFFF	32-bit bank
EPROM	1 Mbyte	000000 0FFFFFF	16-bit bank

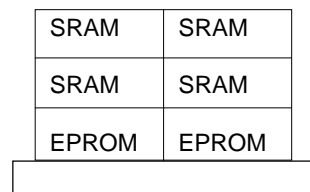


Table 2.3 Memory maps

2.2.4 MEMORY DEVICE SIZES

On both memory banks, SRAM/EPROM device-sizes from 256 Kbit up to 4 Mbit (in byte organization) can be mounted. This gives the following list of usable device-sizes:

SRAM	EPROM
256 kbit	256 kbit
1 Mbit	512 kbit
2 Mbit	1 Mbit
4 Mbit	2 Mbit
	4 Mbit

Table 2.4 Device sizes

Notes:

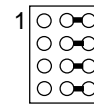
- SRAM can be battery buffered, independent of which bank it is mounted.
- Use low power SRAMs (CMOS) in case of battery buffering.
- 2 Mbit SRAMs are not being manufactured as monolithic chips but 2 Mbit SRAM modules with a JEDEC compatible pin out are available (i.e. Dense-Pac DSP256S8P). To date (march 92), 4 Mbit monolithic SRAMs are not available. Until they are introduced in the market, 4 Mbit SRAM modules can be used (i.e. Dense-Pac DSP512S8P).
- If EPROMs are being used, make sure the battery buffering is NOT SET, otherwise the battery can be discharged prematurely.
- If 1 Mbit EPROMs are used, be sure to use JEDEC types. There are EPROMs available with a Mask ROM compatible pin out which is not compatible to the JEDEC pin out (examples for Mask ROM versions are i.e NEC27C1000, TC571001, Am27C100). These types are not supported by the MPL 4082.

2.2.5 TYPE AND SIZE SELECTION OF MEMORY DEVICES (J14, J15)

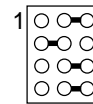
Jumpers J14 and J15 are used for definition of type, size and possible battery buffering of the memory devices mounted on 16-bit bank and 32-bit bank. Jumper J15 defines type, size and battery buffering of the devices on the 16-bit bank. Jumper J14 is the equivalent for the 32-bit bank. Device-type selection (SRAM or EPROM) on jumper J14 and J15 is dependant on the selected memory map. Battery buffering is activated only if a battery source was selected on jumper J13. Fig 2.5 shows the various jumper configurations and is valid for both jumpers, J14 and J15.

SRAM with battery backup:

256 kbit/1 Mbit

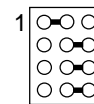


2Mbit/4 Mbit

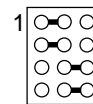


SRAM without battery backup:

256 kbit/1 Mbit

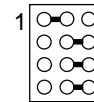


2 Mbit / 4 Mbit

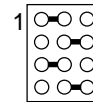


EPROM:

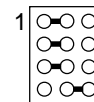
256 kbit



512 kbit/1 Mbit



2 Mbit



4 Mbit

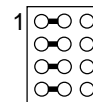


Fig. 2.5 SRAM/EPROM type and size selection

2.2.6 MEMORY ACCESS TIME

The memory access time is determined by the CPU clock frequency and the number of wait states included in read and write accesses. The access logic treats read and write accesses the same way. This means, that both read and write accesses are real 'zero wait state' accesses when set (by jumpers) to 'zero wait state'. SRAM and EPROM access times can be set individually (see 2.2.7) and are not affected by a memory map-swap, thanks to an internal logic that detects which memory map is selected. The access times given below are valid for the internal SRAM and EPROM.

Wait states	Worst case Memory access time for different CPU frequencies		Applicable for memory type
	16 MHz	25 MHz	
0	70ns (100ns)	40ns (55ns)	SRAM/EPROM
1	125ns (170ns)	80ns (100ns)	SRAM/EPROM
2	200ns (250ns)	120ns (150ns)	EPROM
3	250ns (300ns)	150ns (200ns)	EPROM

Table 2.5 Required speed of memory devices

The values in parenthesis denote 'real' access times. With our experience, memory devices with access times as indicated in parenthesis are sufficient even in extended temperature applications.

2.2.7 ON-BOARD MEMORY WAIT STATES (J16)

Wait states for SRAM and EPROM can individually be defined. Swapping the memory map, which means that SRAM and EPROM have to be exchanged mutually, does not affect the wait state definition.

With jumper J16 zero or one SRAM wait states and zero to three EPROM wait states can be set. The jumper in the top position of J16 defines the wait states for SRAM, jumper in the middle and bottom position define wait states for EPROM. Table 2.6 shows the different settings.

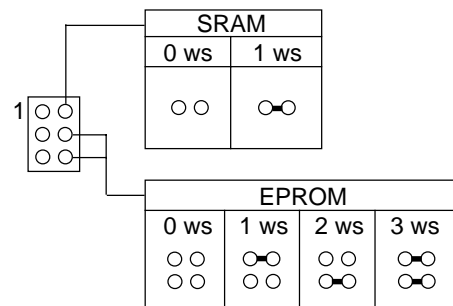


Table 2.6 Wait state selection

2.2.8 MEMORY PIN ASSIGNMENT (U19 - U24)

Memory chips in 28-pin DIL packages must be bottom-aligned (pin 1 of the chip meets pin 3 of the socket).

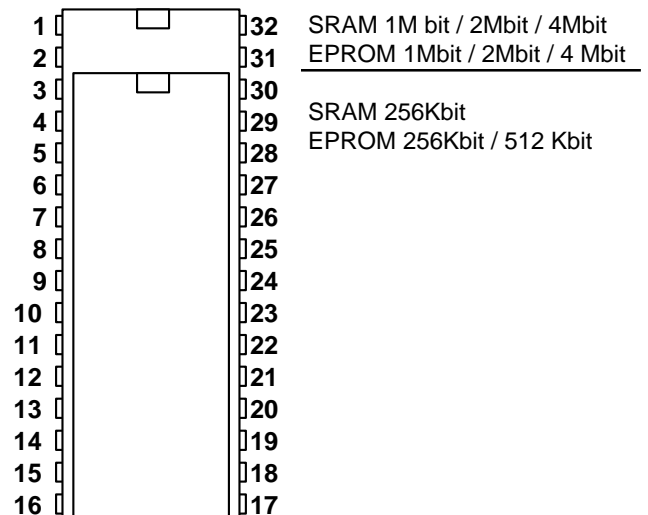


Fig. 2.3 Memory pin assignment

2.3 JUMPER CONFIGURATION AND DESCRIPTION

A lot of functions are implemented on the MPL 4082. Some of these functions have to be set, enabled or disabled by means of jumpers. The locations, the different valid combinations and the meaning of the jumpers are given in the following paragraphs except where they are described in paragraph 2.2 already.

2.3.1 G-96 ADDRESS BUS DRIVERS CONTROL (J5)

The G-96 address bus drivers can be selected on jumper J5 to be always in High-Z or in High-Z only during DMA operations and external HALT conditions. Permanently disabling the address bus drivers reduces current consumption and is especially advised in real Single Board applications. Fig. 2.4 shows the jumper definition.

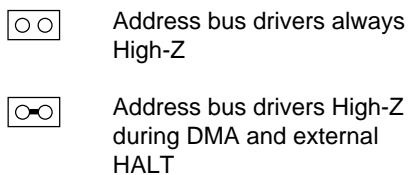


Fig. 2.4 G-96 address bus driver control

2.3.2 ENABLE AND SYCLK CONTROL (J6)

The Enable and SYCLK signals on the G-96 bus can be selected on jumper J6 to be always active or in High-Z during DMA operations and external HALT conditions. See fig. 2.5 for the jumper definition.

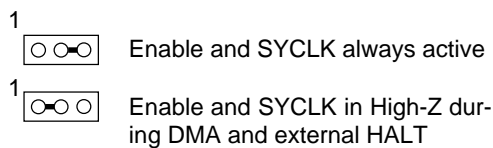


Fig. 2.5 Enable and SYCLK control

2.3.3 ABORT/PWF-G-96 JUMPER (J7)

This 2x2 jumper field has two functions. If a jumper is installed in the upper position as shown below, an active low signal on the G-96 powerfail line releases a level 7 interrupt (NMI). An external abort switch can be connected to the lower position. A closure on this switch will also cause a level 7 interrupt. The interrupt source of a level 7 interrupt can be determined by reading a specially provided interrupt status port, see 3.2.3.

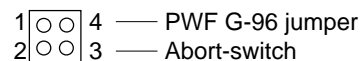


Fig. 2.6 Jumper J7

2.3.4 SYCLK FREQUENCY SELECTION (J8)

The system clock (SYCLK) on the G-96 bus can be set to three different states: The same frequency as the CPU clock, CPU clock divided by two or disabled (always high). In systems where the SYCLK is not used by any bus board, it is advantageous to switch off the SYCLK signal. Noise immunity will be improved (i.e. signal crosstalk and ground bounce). The SYCLK definitions can be set on jumper J8.

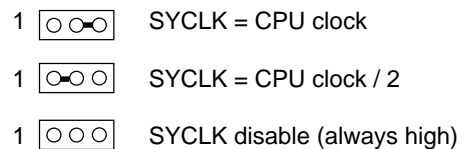


Fig. 2.7 SYCLK frequency selection

2.3.5 RESET (J9)

J9 allows to connect an external reset (restart) switch. A closure on this switch activates a RESET that will be active over the whole system.



Fig. 2.8 Reset switch

2.3.6 CACHE ENABLE/DISABLE (J10)

Jumper J10 is directly connected to the CDIS input of the 68EC020. This input is used to dynamically disable the CPU on-chip cache memory. The CDIS input disables the cache independent of the enable bit in the Cache Control Register and forces the 68EC020 to execute all accesses via its external bus.

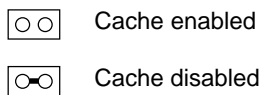


Fig. 2.9 Cache enable/disable

2.3.7 SYNC. OR ASYNC. VPA-RANGE SELECTION (J11)

The lower half of the G-64/96 VPA-range (500 words) is accessible only in the synchronous mode. Access to the upper 500 words can be jumpered to be synchronous or asynchronous.

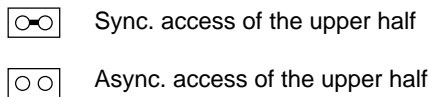


Fig. 2.10 Sync./async. selection of the VPA-range

2.3.8 BATTERY SOURCE SELECTION (J13)

The two possible battery power sources are the on-board lithium battery or a battery connected to the corresponding G-64/96 bus line. If no battery buffering is required, jumper J13 should be removed. Setting a jumper in either position in any case enables the battery buffering for the Real Time Clock. Battery buffering of the on-board SRAM is not yet active, it needs additional setting of jumper J14 or J15.

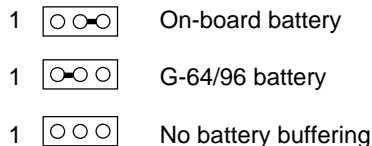


Fig. 2.11 Battery source selection

2.3.9 SOFT-/HARDWARE CLEAR OF THE WATCHDOG (J17)

The watchdog can be jumpered to be cleared by a periodic hardware signal (watchdog is disabled), by a software signal (watchdog is enabled) or to be under software control with the possibility to enable and disable the watchdog by software. Please read paragraph 3.4.2 for more information.

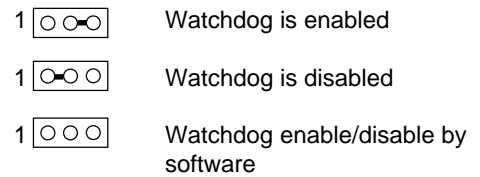


Fig. 2.12 Watchdog mode

2.3.10 4-BIT CONFIGURATION (J18)

A 4-Bit configuration can be set and be read via the Configuration Port. Additionally, the Configuration Port gives information about the selected memory map. For further explanations see 3.4.1.

Each jumper set will be read as a '0', each jumper left open will be read as a '1'.

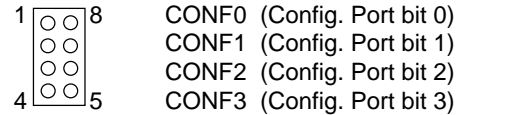


Fig. 2.13 4-bit configuration

2.3.11 2-BIT CONFIGURATION (J19)

A 2-Bit configuration can be set and be read via DUART input ports 4 and 5. A jumper set will be read as a '0', a jumper left open will be read as a '1'.

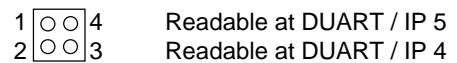


Fig. 2.14 2-bit configuration

2.3.12 SIMM MODULE INTERRUPT (J20)

The SIMM microedge connector (MLX-bus) provides an active low interrupt output line. This line is internally connected to interrupt level 4 (together with VIA1 and VIA2) and at the same time to the DUART input port 3 ('IRQ-Flag'). Jumper J20 offers the possibility of disconnecting the SIMM Module interrupt from interrupt level 4 by removing the jumper. The IRQ-Flag bit at the DUART input port is still available.

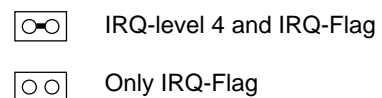


Fig. 2.15 Jumper J20

2.4. CONNECTORS

2.4.1 LOCAL EXTENSION BUS (J4)

The MPL 4082 is equipped with a 30-pin SIMM microconnector for the installation of small and low cost peripheral devices. See part 5 for complete details on the local extension bus specifications.

2.4.2 DUAL RS-232 10POL CONNECTOR (J2)

J2 allows the connection of two serial RS-232 channels with hardware handshake. The communication device on the MPL 4082 is a DUART 68C681. All RS-232 output signals have a typical voltage range of ± 9 Volts. The following table shows the pin out of the 10-pin connector.

Pin number	Signal
1	TxD A
2	RxD A
3	RTS A
4	CTS A
5	GND
6	TxD B
7	RxD B
8	RTS B
9	CTS B
10	GND

Table 2.6 RS-232 connector

Suffix "A" denotes Channel A, suffix "B" denotes channel B. "A" and "B" correspond to the denotation used in the device data sheet of the communication controller 68C681.

2.4.3 I/O LINES 50POL CONNECTOR (J3)

J3 is a 50-pin connector with 40 VIA I/O lines (four VIA-Ports including all handshake signals), 8 SIMM Module I/O lines and 1 VCC- and 1 GND-line. Table 2.6 shows the pin out of connector J3. Pins 1 to 20 are the I/Os of VIA1 (U30), pins 21 to 40 are the I/Os of VIA2 (U31).

Pin number	Signal	Pin number	Signal
1,21	PA0,PA0	16,36	PB5,PB5
2,22	PA1,PA1	17,37	PB6,PB6
3,23	PA2,PA2	18,38	PB7,PB7
4,24	PA3,PA3	19,39	CB1,CB1
5,25	PA4,PA4	20,40	CB2,CB2
6,26	PA5,PA5	41	SIMM2
7,27	PA6,PA6	42	SIMM3
8,28	PA7,PA7	43	SIMM4
9,29	CA1,CA1	44	SIMM5

Pin number	Signal	Pin number	Signal
10,30	CA2,CA2	45	SIMM6
11,31	PB0,PB0	46	SIMM7
12,32	PB1,PB1	47	SIMM8
13,33	PB2,PB2	48	SIMM9
14,34	PB3,PB3	49	VCC(+5V)
15,35	PB4,PB4	50	GND

Table 2.8 I/O lines connector

2.5 INDICATORS

2.5.1 STATUS LED

The MPL 4082 provides a status indicator LED. Whenever the indicator is "on", something is wrong.

The red LED D8 will be on permanently if:

- the power (VCC) in power-up never exceeds 4.80V
- the power (after a correct power-up) drops below approx. 4.60V
- the microprocessor is in the HALT-state (i.e. double bus error or HALT G-96)

The LED will periodically turn on (RESET) and off with approx. 3 Hz if the watchdog time out had been released as a result of a missing clear signal (watchdog is enabled).

2.5.2 OPTIONAL LEADS

On the solder side of the MPL 4082 three chip LEDs can be mounted (located at the upper card edge, above the string '<C> 1991 by MPL AG ...').

For each LED a series resistor of 330 Ω is already provided. This results in a diode forward current of approx. 8mA. The LEDs are controlled by the DUART 68C681 outputs OP5 - OP7. Programming an output to "0" lights the corresponding LED. See fig. 2.16 for details and read paragraph 3.4.4 for the bit definition of the DUART output port.

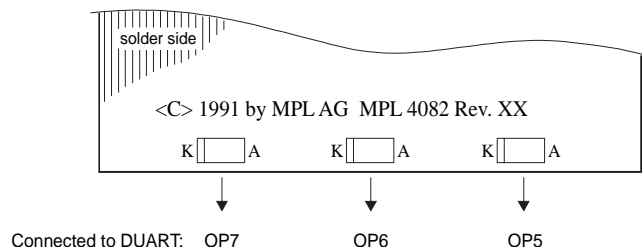


Fig. 2.16 LEDs (optional)

Note:

Chip LEDs with almost equal luminous intensities are available from Citiled (example): CL-150SR (red), CL-150Y (yellow), CL-150FG (fresh green).

3. OPERATION

3.1 BASIS

This section outlines some basic operation and function principles of the MPL 4082.

3.1.1 VECTOR BASE REGISTER

The 68EC020 offers a vector base register. This register provides the base address of the exception vector table. The displacement of an exception vector is added to the value in this register to access the vector table. With this, it is possible to locate the EPROM bottom address permanently at \$000000. On the MPL 4082, the value programmed to the vector base register usually is identical to the start address of the SRAM (\$100000 or \$200000, dependent on the selected memory map).

3.1.2 ACCESS MODES

The MPL 4082 supports both asynchronous and synchronous data transfers between CPU and memory/peripheral. Asynchronous transfers need to be terminated by a Data Acknowledgment (DTACK) signal. All transfer modes supported on the MPL 4082 are listed in Table 3.1.

Read-Modify-Write cycles are correctly supported in both asynchronous and synchronous mode provided that TAS instructions only are used (CAS and CAS2 instructions will not be executed 'undivided').

Device	Data transfer	DTACK origin
Int. Memory	async.	internal
DUART	async.	internal
VIAs	sync.	—
Int. Ports	sync.	—
RTC	sync.	—
SIMM Module	sync.	—
G-64/96 VPA	sync. and/or async.	(external)
G-64/96 VMA	async.	external

Table 3.1 Operational modes

3.1.3 ADDRESSING OF PERIPHERAL DEVICES

Pay attention when accessing on-board peripherals: On the MPL 4082, all peripheral devices are 8-bit wide and connected to the upper middle data byte (D23 - D16) of the CPU data bus, but are defined to be 16-bit ports (word wide)! Therefore use odd addresses only and increment the addresses by 2 to get the next contiguous address. This addressing pattern was chosen to achieve a high addressing map compatibility to the MPL-4080, an earlier MPL Single Board Computer module. Accessing 8-bit peripherals via the G-64/96 bus, which is also a 16-bit port, is similar. These peripherals are internally

connected to D23 - D16 (odd, G-64/96 data lines D7-D0) or to D31 - D24 (even, G-64/96 data lines D15-D8). In each case, increment the addresses by 2 to get the next contiguous address.

3.1.4 BUS ERROR LOGIC

In a 68EC020 system, each asynchronous access to any peripheral or any memory device has to be terminated by an acknowledgment signal (/DTACK). The device itself or a special decode logic has to deliver this acknowledgment, otherwise the microprocessor will forever hold the initiated bus cycle active. To prevent this, an on-board bus error logic aborts such a data transfer after approx. 20µsec and releases a bus error (BERR).

Note:

On the MPL 4082 the BERR signal is not accompanied by a HALT signal. Thus the 68EC020 will not initiate a rerun bus cycle. The bus error has to be handled in software. A renewed bus error during the exception processing will be treated as a catastrophic error (double bus fault) and the 68EC020 will automatically enter the HALT-state and remain there until reset.

3.2 INTERRUPTS

3.2.1 INTERRUPT LOGIC

The relation between interrupt source, interrupt mode and interrupt level is hard-wired and can not be altered. Interrupt levels 1 to 6 are level sensitive while level 7 is transition sensitive. The sources of level 7 interrupts can be detected individually by consulting the interrupt status port (see next two paragraphs).

Level	Mode	Source
1	auto-vect.	G-64/96 IRQ1 (or G-64 IRQ)
2	auto-vect.	G-64/96 IRQ2 (or G-64 FIRQ)
3	vectored	G-96 IRQ3
4	auto-vect.	VIA1 & VIA2 & SIMM Module
5	vectored	G-96 IRQ5
6	vectored	DUART
7	auto-vect.	Powerfail MPL 4082 Abort Switch NMI G-64/96 Powerfail G-64/96 (enable/disable by jumper J7)

Table 3.2 Interrupt logic

Note:

Powerfail MPL 4082 and Powerfail G-64/96 are wired together and are treated as a single interrupt source.

3.2.2 LEVEL 7 INTERRUPT PRINCIPLES

Attention has to be paid to level 7 interrupts since there are various interrupt sources (i.e. Power Fail and Abort) that cannot be cleared by the interrupt handler routine. The MPL 4082 offers an on-board interrupt status port that allows to detect the level 7 interrupt source.

A special circuit connects all level 7 interrupts sources together and transforms any (active) level 7 interrupt to a pulse of approx. 300µsec length. This means, that any level 7 interrupt will be de-activated after approx. 300µsec independent of actually being still active or not. This mechanism prevents the interrupt handler routine from being dead-locked by a non-clearable level 7 interrupt. The status of this pulse can be detected in the interrupt status port as well as the level 7 interrupt sources. As long as the pulse is active, renewed level 7 interrupts will not be processed. The function principle of the pulse generator is very similar to a 'retriggerable monoflop'.

The interrupt handler routine should monitor the interrupt status port for two reasons. First to see which level 7 interrupt source released the interrupt in progress. Second to detect the moment where the interrupt handler routine can be quitted (RTE or MOVE to SR instruction). If a RTE or MOVE to SR instruction is executed and the level 7 pulse is still active, then possibly a level 7 interrupt will be released again. This is due to the fact, that the CPU automatically re-sets the internal interrupt priority mask level to the level as it was before the interrupt was recognized. If this level is not equal to level 7, then a level 7 interrupt will be released.

Refer to Fig. 3.1 for better understanding.

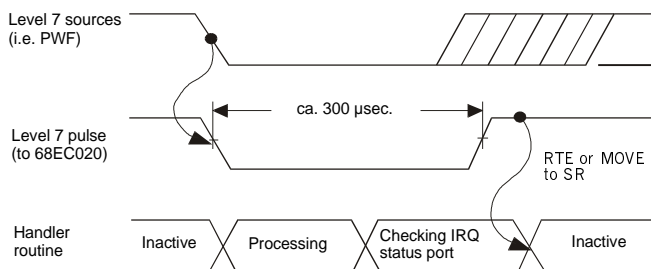


Fig. 3.1 Level 7 interrupt work-out

3.2.3 LEVEL 7 INTERRUPT STATUS PORT

This port reflects the actual state of the different level 7 interrupt sources as well as the state of the level 7 pulse. There are three possible interrupt sources: G-64/96 level 7 interrupt (NMI), on-board Abort on jumper J7, G-64/96 (external) and MPL 4082 (internal) Powerfail. The G-64/96 Powerfail line can be connected or disconnected on jumper J7. The level 7 interrupt pulse is the common input to the 68EC020 and has a fixed length. Table 3.3 shows the bit definition of the interrupt status port.

Byte read access to address \$3304B1 (IRQ status port)

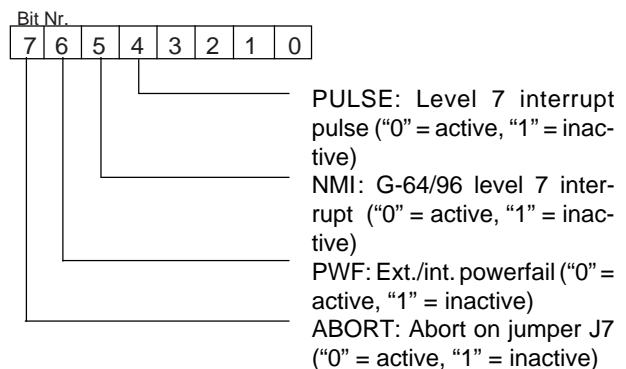


Table 3.3 Interrupt status port

3.3 MEMORY MAP

CPU address	G-96 bus address [see (1)]	Space name	Sync./ Async.	16-bit port even (D31 - D24)	16-bit port odd (D23 - D16)	32-bit port (D31 - D0)	Comment
FFFFFF 400000	7FFFFFF 200000	VMA G-64/96	Async.	X	X		
3304DF 3304C0		WD-Switch	Sync.		X		see (2)
3304BF 3304B0		IRQ stat. Port	Sync.		X		
3304AF 3304A0		Config. Port	Sync.		X		
33049F 330480		SIMM Module	Sync.		X		
33047F 330460		VIA2	Sync.		X		
33045F 330440		VIA1	Sync.		X		
33043F 330420		WD-Clear	Sync.		X		see (2)
33041F 330400		RTC	Sync.		X		see (3)
3207FF 320400	1903FF 190200	VPA G-64/96	Sync./ Async.	X	X		selectable
3203FF 320000	1901FF 190000	VPA G-64/96	Sync.	X	X		
3007FF 300400		DUART	Async.		X		

32-bit wide EPROM / 16-bit wide SRAM (J12 = 'out')

2FFFFFF 200000		RAM	Async.	X	X		
1FFFFFF 000000		EPROM	Async.			X	

16-bit wide EPROM / 32-bit wide SRAM (J12 = 'in')

2FFFFFF 100000		RAM	Async.			X	
0FFFFFF 000000		EPROM	Async.	X	X		

Table 3.4 Memory map

Notes:

- (1) CPU address lines A1 - A23 drive the G-96 address bus lines A0-A22. Bus line A23 is always low. Thus a G-64/96 access is actually a word-access. Therefore you have to transform the addresses when accessing G-64/96 devices: the effective bus addresses are listed in this column.
- (2) Read paragraph 3.4.2 for clarity
- (3) Only the lower 4 bits are used (D19 - D16)

3.4 DEVICE DESCRIPTION

In this section, the devices of the MPL- 4082 will be described. Sometimes the sentence “see the data sheet.....for more information” appears. The data sheets referred to will usually give you more accurate information about the circuits than could possibly be given within the scope of this manual.

3.4.1 CONFIGURATION PORT

Reading the Configuration Port gives information about the 4-bit configuration set on jumper J18 and the memory map set on jumper J12. Jumper J12 for example can be used for correct initialization of the vector base register after reset. Table 3.5 shows the bit definition of the Configuration Port.

Byte read access to address \$3304A1 (config port)

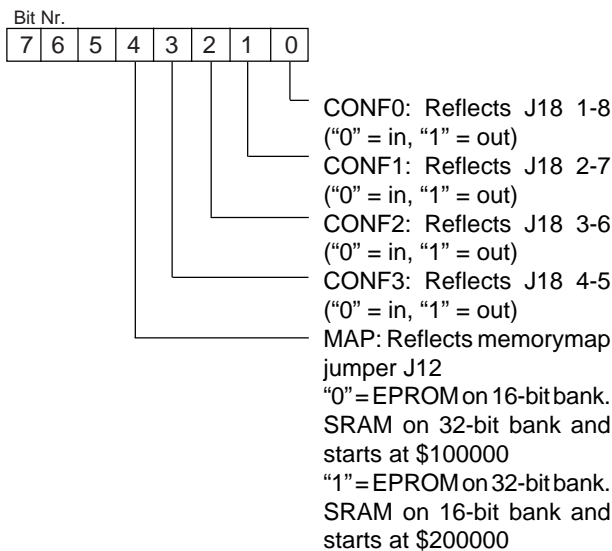


Table 3.5 Configuration Port

3.4.2 WATCHDOG (U34)

The watchdog circuit has to be cleared periodically to prevent watchdog time out and system reset. On the MPL 4082 there are two possible clear-sources. The first clear-source is a periodical hardware signal (CPU E-signal) and clearing the watchdog this way is called HW-C (hardware-clear). The second clear-source is a short pulse served by the user software that should clear the watchdog within the time out period of 100ms. Clearing the watchdog with a software pulse is called SW-C (software-clear).

3.4.2.1 WATCHDOG ALWAYS DISABLE

Placing jumper J13 to the corresponding position disables the watchdog since it is set to HW-C. This mode will be chosen when the watchdog safety function is not desired or during software development.

3.4.2.2 WATCHDOG ALWAYS ENABLE

Placing jumper J13 to the corresponding position enables the watchdog and sets it to SW-C. The watchdog has to be cleared by a software pulse (generated by a read or write access to the WD-Clear address). This mode is applicable only if the software structure guarantees clearing of the watchdog within the time out period of 100ms.

If the watchdog is not cleared within the time out period, a system reset will be performed. After an additional 100ms, reset will be withdrawn (becomes inactive) to give the system a chance to carry out a new start-up. This sequence will be repeated periodically until the watchdog is cleared again.

Generating the watchdog-clear pulse:

Byte read or write access to address \$330421 (WD-Clear), data is irrelevant

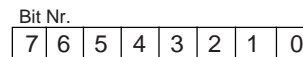


Table 3.6 WD-Clear

Note:

During a HALT condition issued from the corresponding G-64/96 signal line, the watchdog is automatically in HW-C mode. This prevents an unnecessary watchdog time out (the CPU is forced to inactivity).

3.4.2.3 WATCHDOG ENABLE/DISABLE BY SOFTWARE

If jumper J13 is placed to the watchdog enable/disable position, after reset the watchdog is always set to HW-C. This is helpful in applications where boot and start-up procedures are very long and the watchdog cannot be cleared during this time. After start-up, the watchdog can be programmed to SW-C and henceforth has to be cleared by a software pulse (WD-Clear, see above). If necessary, the watchdog can be re-programmed to HW-C by software.

Switching the watchdog to SW-C is simply done by a read or write access to the WD-Switch address (no TAS instruction). Switching back the watchdog to HW-C uses the same mechanism but works only with TAS instructions.

How to switch from HW-C to SW-C and back is shown in Table 3.7. Fig. 3.2 illustrates a sequence of watchdog switching.

Switching to SW-C:

Byte read or write access to address \$3304C1 (WD-Switch), no TAS instruction, data is irrelevant

Bit Nr.							
7	6	5	4	3	2	1	0

Switching to HW-C:

Byte read or write access to address \$3304C1 (WD-Switch), TAS instruction only, data is irrelevant

Bit Nr.							
7	6	5	4	3	2	1	0

Table 3.7 Programming HW-C or SW-C

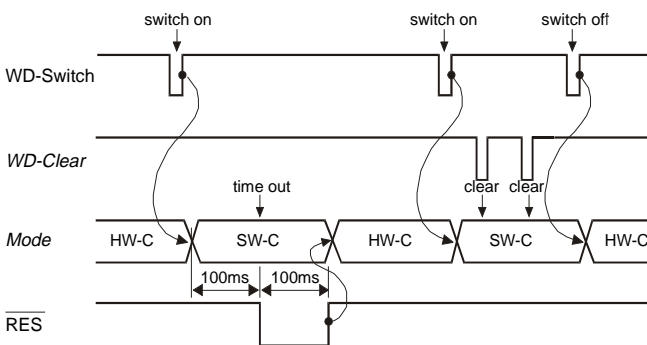


Fig. 3.2 Watchdog switching sequence

Note:

During a HALT condition issued from the corresponding G-64/96 signal line, the watchdog is automatically in HW-C mode. This prevents an unnecessary watchdog time out (the CPU is forced to inactivity).

Power-up/down reset, manual reset and time out reset always set the watchdog to HW-C. A reset issued by the CPU itself (RESET instruction) does not affect the setting!

3.4.3 POWERFAIL (U34)

To guarantee operation of the MPL 4082 after power-up, the power (VCC) has to rise above 4.80V. Otherwise the system reset will stay active.

In power-down (powerfail situation) the MPL 4082 will run through following stages:

4.70V: When the power drops below this voltage level, a SAVE-function releases a level 7 interrupt (PWF). This gives the possibility of saving data to a battery buffered RAM before a destructive system reset will become active.

4.60V: When the power drops below this voltage level, a system reset will be released and lasts until the voltage has risen over 4.80V again. An active system reset disables the access to the RAM.

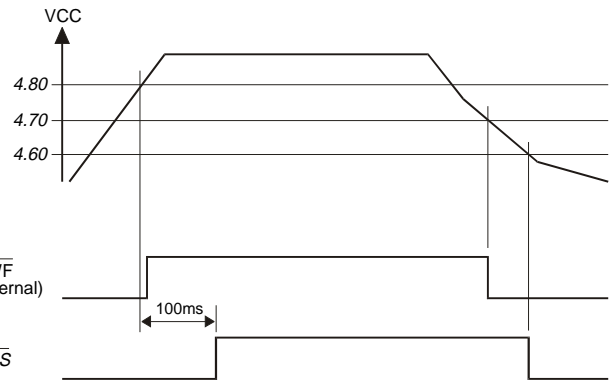


Fig. 3.3 Powerfail reaction

For more information about watchdog and powerfail, see data sheet H6060 from EM Microelectronic-Marin.

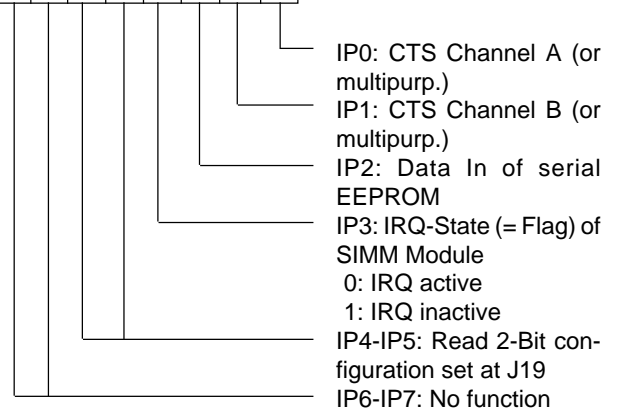
3.4.4 SERIAL INTERFACE & SPECIAL PORTS (U32)

The Dual Universal Asynchronous Receiver/Transmitter 68C681 is used for the serial interface. It consists of two serial channels with independent programmable baud rate from 50 to 38400 Baud. Each channel can be used as a 5-wire communication interface (TxD, RxD, RTS, CTS and GND). The vectored interrupt and the 16 Bit counter/timer are two additional features. The DUART is clocked with a 3.6864 MHz crystal oscillator.

Besides these features there is an 8-Bit Output Port and a 6-Bit Input Port which can be used partly as multipurpose I/Os. Some of these port-bits are used for the serial communication, some have special functions within the MPL 4082. Both ports are described below.

Input Port:

Bit Nr.							
7	6	5	4	3	2	1	0



Output Port:

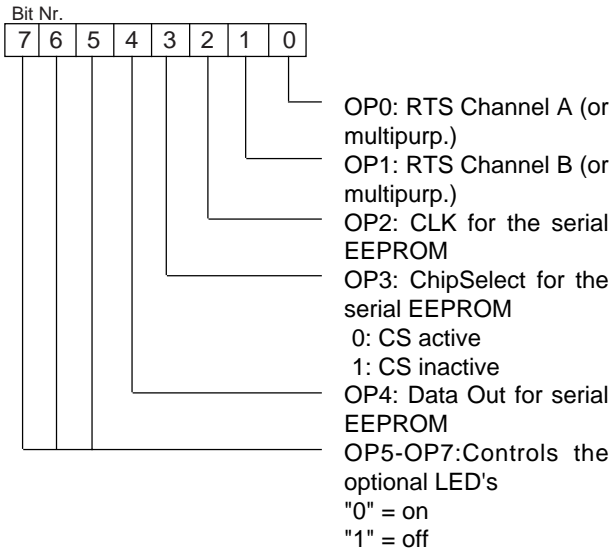


Table 3.8 DUART ports

All bits of the output port are "1" after reset.

See the data sheet from Motorola (MC68681), EXAR (XR-68C681) or Philips (SCC68692) for a detailed description of the DUART.

3.4.5 PARALLEL INTERFACE & TIMERS (U30, U31)

The devices used for the parallel interface are two VIA 65SC22. VIA1 is located at U30 and VIA2 at U31. These devices offer different modes of operation. In total four parallel ports (8 bits each) with handshake signals (2 each) are provided. The 4 timers can be used for time-slice generation in a real-time operating system, to count pulses, and generate frequencies.

See the data sheet from CMD (California Micro Devices, 65SC22) or from Rockwell International (65NC22) for a detailed description.

Note:

The I/O's of both VIAs are directly connected to connector J3. There are no additional drivers provided. For some applications (i.e. centronics interface), external driving of the I/O's might be necessary.

3.4.6 SERIAL EEPROM (U35)

The mounted 3-wire serial EEPROM (location U35, part number 93C46) is a 1024 bit memory device, organized in 64 registers of 16 bits each.

The serial EEPROM can be programmed, read or written via the DUART ports (see 3.3.4). The ChipSelect (CS, active high) is inverted since the DUART output OP3 is high after reset. Fig. 3.3 illustrates the interconnection DUART <—> serial EEPROM.

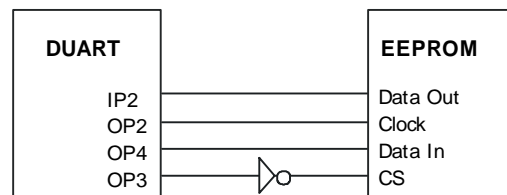


Fig. 3.4 Interconnection DUART- EEPROM

Important Note:

Comparing EEPROM devices with the part number '93C46' shows differences in the programming sequence: Some devices do not need an Erase and/or Erase All instruction prior to a Write and/or Write All instruction since they erase automatically on Write/Write All instructions. MPL cannot guarantee to generally equip the MPL 4082 either with devices with or without automatic erase feature. Therefore, the 3-wire serial EEPROMs equipped on the MPL 4082 require an Erase and Erase All cycle prior to the Write and Write All instruction! Some of the manufactures listed below offer devices with automatic erase feature. However, they all have to be programmed the conservative way. Following data sheets can be consulted: Samsung (KM93C46), Hyundai (HY93C46), SGS-Thomson (ST93C46A), Catalyst Semiconductor (CAT93C46), OKI (MSM16811RS), Atmel (AT93C46), National Semiconductor (NMC93C46).

3.4.7 REAL TIME CLOCK (U36)

The real time clock is the RTC72423 from Seiko. The circuit is clocked with a integrated 32'768 Hz crystal oscillator and offers time and date functions. Only the lower four data bits are used and connected.

For more information see the data sheet RTC72423 from Seiko (or the data sheet of RTC72421 which is the DIL-version of the functional identical chip).

Note:

The STD.P-output (pin 1) is not used.

3.5 G-64/96 BUS DESCRIPTION

3.5.1 G-64/96 BUS INTERFACE

The bus interface of the MPL 4082 represents a full support of the G-96 (and G-64) bus. Synchronous and asynchronous 8/16 Bit peripherals in the predecoded VPA-range (1 kword) and up to 12 Mbyte in the asynchronous VMA range can be addressed. Two vectored and three auto-vectored interrupts are supported.

All bus drivers are of 48mA type and meet the specifications of a hard-terminated G-64/96 backplane (330 Ω /470 Ω networks at each end of the backplane). Table 3.9 shows the signals provided on the G-96 bus connector:

Signal	Type (1)	Description	Comment
D0 - D15	I/O	Data lines	
A0 - A23	OUT	Address lines	A23 is always low
/VPA	OUT	Valid peripheral signal	valid within 1 kword
/VMA	OUT	Valid memory address	valid for addresses • \$400000
/DS0, /DS1	OUT	Data strobes	valid during VPA, VMA and IACK cycles
R/W	OUT	Read/write signal	
/BRQ, /BGACK	IN	DMA control signals	see 3.5.3 for more information
/BG	OUT	DMA control signal	see 3.5.3 for more information
/IRQ1 - 3, /IRQ5, /NMI	IN	Interrupt lines	
/RES	OC OUT	Reset (2)	
E	OUT	CPU Enable	1/16 of CPU clock
SYCLK	OUT	System clock	1/1 or 1/2 of CPU clock
/IACK	OUT	Interrupt acknowledge	for vectored levels 3 and 5
/BERR	IN	Bus error	wired-and with the on-board BERR
/HALT	IN	CPU halt	all G-96 outputs go High-Z
/DTACK	IN	Data acknowledge	for asynchronous data transfer
/PWF	IN	Powerfail (3)	wired-and with the on-board PWF
/Page	OUT	Memory expansion	connected to CPU address line A17
CHOUT	Passive	Daisy chain out	pulled up to +5V (4.7k Ω)

Table 3.9 G-96 bus signal description

Notes:

- (1) Seen from the MPL 4082
- (2) RESET is an open collector output but NOT bidirectional.
- (3) In older G-64 bus designs (prior to 1984), pin 29a is a -5V INPUT and has to be open. Since then, pin 29a has changed its function and has now become a Power Fail input and is supported by the MPL 4082 (level 7 interrupt).

For more details refer to the G-64/G-96 SPECIFICATIONS MANUAL Rev.3.

3.5.2 ASYNCHRONOUS G-64/96 ACCESSES

Asynchronous accesses via the G-64/96 bus have to be acknowledged by an acknowledgment signal (DTACK) to indicate that the access can be terminated. If the DTACK is not negated within a defined time after the access had been terminated by the CPU, the next access can be seen as a 'zero wait state' access. To prevent erroneous behavior in such a case, the MPL 4082 starts G-64/96 accesses only when the bus DTACK is not (no longer) active. The start of the accesses can not be delayed for an infinite time, the on-board bus error logic aborts such locked accesses after approx. 20µsec. On-board accesses are not affected by this mechanism and will be executed without delay and with the number of wait states as defined.

To get the maximum speed out of G-64/96 memory or peripheral boards, some users like to know the CPU response time of 'DTACK active to DS0/DS1 negated' (which might be helpful when optimizing write accesses).

A second parameter of interest, especially in read cycles, is the time 'DTACK active before data valid'. According to the G-64/96 specification, DTACK should become active after data is valid. Regardless of that fact, on the MPL 4082 DTACK can become active a defined time before data is valid.

See fig. 3.5 for timing details.

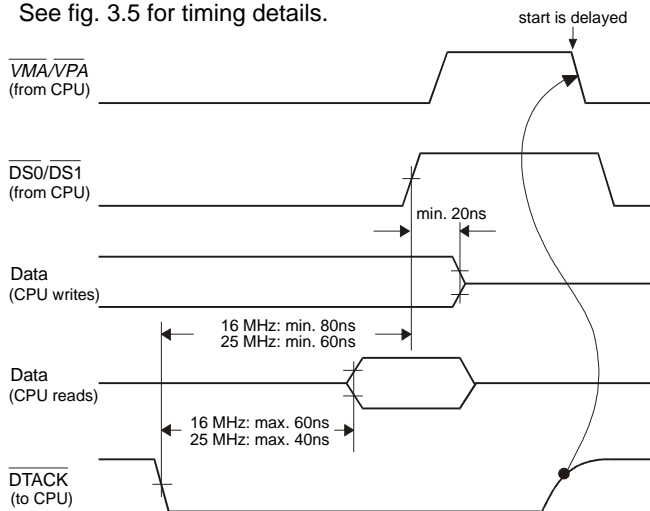
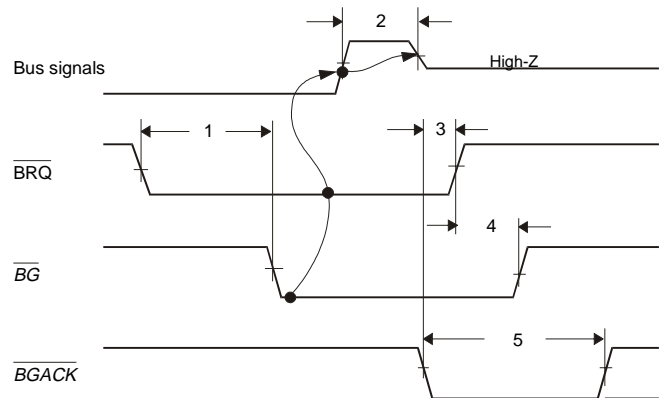


Fig. 3.5 CPU response time and access lock

3.5.3 BUS ARBITRATION

The MPL 4082 offers bus arbitration capability. Three control signals are dedicated to that purpose: /BRQ, /BG and /BGACK. If a device requests the G-96 bus, the bus arbitration timing of Fig. 3.6 has to be met. For a correct timing, the bus requesting device must monitor several signals, i.e. VMA, VPA and DTACK have to be negated before the bus requesting device is allowed to release the /BGACK signal.



Nr.	Description	Min [ns]	Max [ns]
1	/BRQ low to /BG low	60	220
2	/BRQ, /BG low and VMA, VPA inactive to bus high-Z		50
3	/BGACK low to /BRQ high	0	
4	/BRQ high to /BG high		35
5	/BGACK low width	60	

Fig. 3.6 Bus arbitration timing

4. COPROCESSOR PIGGY BACK

The 68881/68882 provide a logical extension to the 68EC020 integer data processing capability. The 68881/68882 execute instructions fully concurrent, feature a full set of trigonometric and transcendental functions and have full conformance to the ANSI-IEEE 754 standard. The 68882 is a pin and software-compatible upgrade of the 68881, with an optimized processor interface that provides over 1.5 times the performance of the 68881 at the same clock frequency.

The MPL 4082 can optionally be equipped with the floating-point coprocessor 68881/68882 by the use of a small and compact piggy back. This will increase computing and calculating power of the MPL 4082 by factors.

The coprocessor piggy back connects the 68EC020 to the 68881/68882 in full 32-bit data width. 68EC020 and 68881/68882 run on the same clock frequency of 16 MHz or 25 MHz. The PCB offers a 13x13 PGA-socket for re-insertion of the 68EC020 and a 68 pin PLCC-socket for insertion of the 68881/68882 (PLCC devices!). A fast chip select decode makes possible 68881/68882 accesses without unnecessary wait states. When the PCB is mounted, the total height of the MPL 4082 is still below 16mm. This allows slot-by-slot insertion of G-64/96 boards in a standard bus system.

The piggy back without 68881/68882 can be ordered from MPL AG with ordering number MPL-FPU-1.

PCBs equipped with a 68882 (16 MHz or 25 MHz) are available on request.

5. MLX LOCAL EXTENSION BUS

The MPL 4082 can be customized to a great extent through the use of its local extension bus. Although the notion of a local bus is now very common in the industry, the board's Mpl Local eXtension bus (MLX) is designed to allow the easy addition of very simple and very low cost peripheral devices. A selection of MLX add-on modules is already available and others may be custom designed by MPL AG or the user, in order to adapt the MPL 4082 to a specific requirement.

5.1 SIGNAL DESCRIPTION AND PIN ASSIGNMENT

The MLX bus uses a 0.1 inch centerline, single row 30-pin MICRO-EDGE SIMM connector from AMP. Signal description and pin assignment are shown in table 5.1

Pin	Signal	Type	Description
1	VCC	PWR	+5V power
2	GND	PWR	Ground
3	D0	I/O	Data line
4	D1	I/O	Data line
5	D2	I/O	Data line
6	D3	I/O	Data line
7	D4	I/O	Data line
8	D5	I/O	Data line
9	D6	I/O	Data line
10	D7	I/O	Data line
11	A1	IN	Address line
12	A2	IN	Address line
13	A3	IN	Address line
14	A4	IN	Address line
15	/CS-MOD	IN	Module Select
16	E	IN	Enable signal
17	R/W	IN	Read/Write control
18	/RES	IN	Reset
19	/IRQ	OUT (OC)(2)	Interrupt
20	GND	PWR	Ground
21	SIMM0	I/O	Multi-purpose I/O(1)
22	SIMM1	I/O	Multi-purpose I/O(1)
23	SIMM2	I/O	Multi-purpose I/O
24	SIMM3	I/O	Multi-purpose I/O
25	SIMM4	I/O	Multi-purpose I/O
26	SIMM5	I/O	Multi-purpose I/O
27	SIMM6	I/O	Multi-purpose I/O
28	SIMM7	I/O	Multi-purpose I/O
29	SIMM8	I/O	Multi-purpose I/O
30	SIMM9	I/O	Multi-purpose I/O

Table 5.1 MLX bus pin assignment

Notes:

- (1) Signals SIMM0 and SIMM1 are not connected on the MPL 4082 and can not be used as I/Os. Signals SIMM2-SIMM9 are wired to connector J3.
- (2) Open collector output signal

5.2 SIGNAL TIMING

The MLX bus supports only synchronous cycles. The timing specification given in Fig.5.1 and Table 5.2 assumes that synchronous peripheral devices will be used on the module. Table 5.2 shows two columns. The first shows the minimum times when using 1 MHz peripheral devices (68EC020 with 16 MHz), the second shows the corresponding timings when using 2 MHz peripheral devices (68EC020 with 25 MHz).

Timing	Description	Speed of peripheral device	
		1 MHz Min.(ns)	2 MHz Min.(ns)
1	Enable pulse width high	450	220
2	Address lead time	220	100
3	Address hold time	20	20
4	ChipSelect lead time	170	70
5	ChipSelect hold time	20	10
6	Write control lead time	220	100
7	Write control hold time	20	20
8	Data setup time write	430	200
9	Data hold time write	30	10
10	Data setup time read	80	50
11	Data hold time read	10	10

Table 5.2 MLX bus timing information

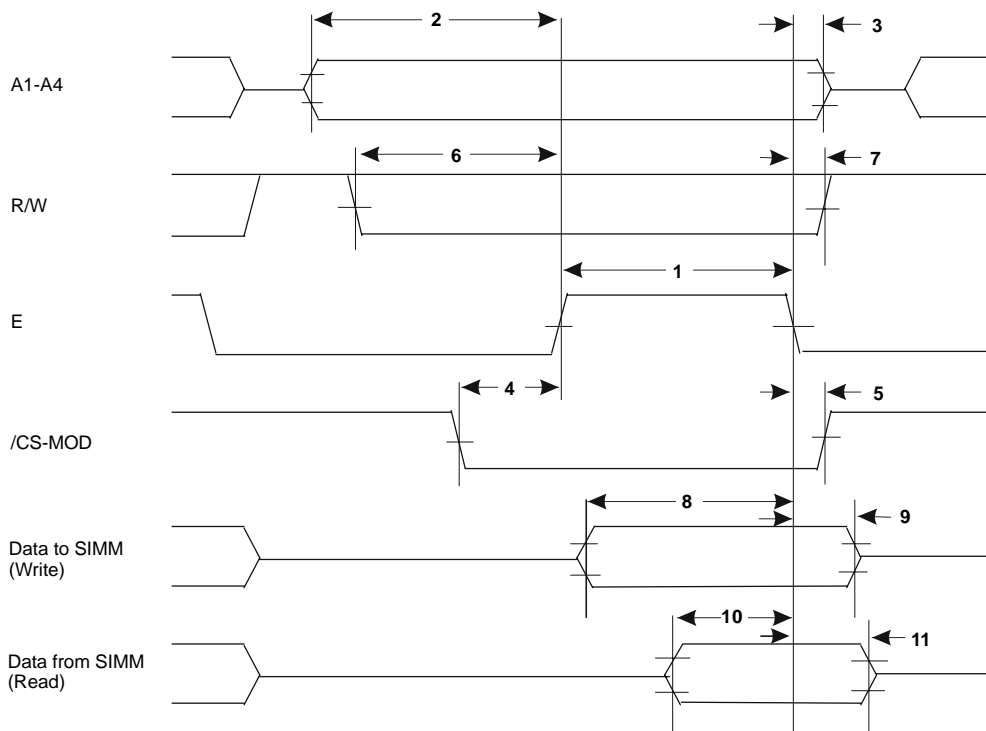


Fig. 5.1 MLX bus timing diagrams

5.2 MLX BUS MECHANICAL DIMENSIONS

Figure 5.2 shows the typical dimensions of a MLX expansion module.

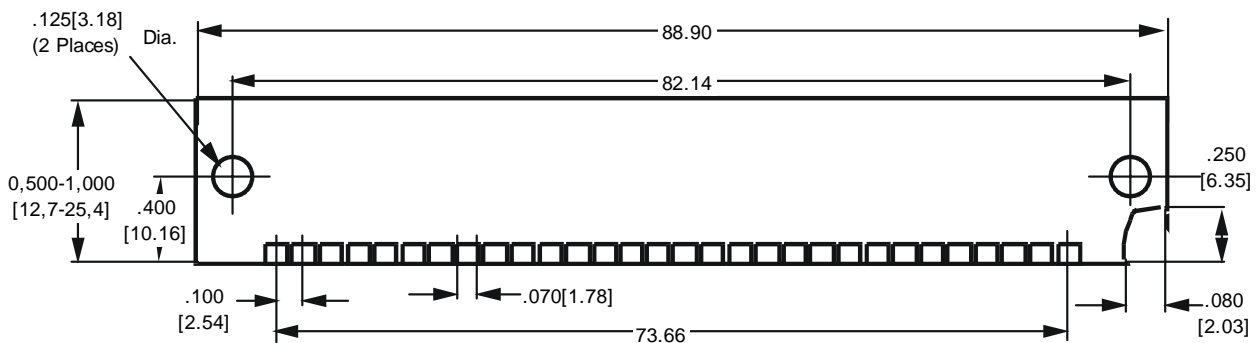


Fig 5.2 MLX bus module mechanical dimensions

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